A 0.5-V Ultra-Low-Power OTA With Improved Gain and Bandwidth

M. Razzaghpour and A. Golmakani

Abstract — In the context of ultra-low-power and ultra-low-voltage operational transconductance amplifiers (OTAs), there is the inconvenience of low unity-gain frequency and DC gain. In this paper, we presented a 0.5-V improved ultra-low-power OTA using the transistors operate in weak inversion. The proposed topology based on a bulk-driven input differential pair employed an under-weak-inversion gain-stage in the Miller capacitor feedback path to improve the “pole-splitting” effect. Simulations in a standard 0.18 µm CMOS process resulted on considerable enhancement in the unity-gain bandwidth and the DC gain as well. The topology presents rail-to-rail input and output swings and consumes only 1 µW.

Keywords: Bulk-Driven Differential Pair, Full Swing, Miller Compensation, Operational Transconductance Amplifier (OTA), Right Half-plane Zero Control, Ultra-Low-Voltage, Ultra-Low-Power.

I. Introduction

As the feature size of modern CMOS processes scale down, the maximum allowable power supply continuously decreases. The main drawback on implementing low-voltage CMOS circuits is the threshold voltage which does not scale down as the same rate as power supply reduction. Therefore, some circuit structures become obsolete and there is the need for alternative architectures which is able to satisfy a wide voltage range in order to achieve a desirable signal-to-noise ratio [1]-[5].

Unquestionably, the weak inversion region of a MOS transistor is suitable for implementing ultra-low-power circuits. However, under weak inversion the unity-gain bandwidth (UGBW) will be limited due to the extremely low currents. In the context of low-voltage and low-power design, one of the most suitable structures is the bulk-driven differential pair, which allows a large input signal swing [6]-[8]. However, since the bulk-source transconductance $g_{sb}$ is smaller than the gate-source transconductance $g_m$ and owing to the extremely low currents, the gain-bandwidth product (GBW) will be considerably limited [9].

Although several solutions have been reported based on bulk-driven structures [8], [10], [11], [12], [13], all of them present the drawback of either a reduced open loop gain or an undesirable unity gain frequency. This paper demonstrates an alternative low-area approach without the use of additional circuit or extra power consumption.

In this paper, an ultra-low-power and ultra-low-voltage OTA based on a bulk-driven input differential pair is modified to be able to overcome the problem of low DC gain and unity-gain bandwidth. The open loop gain and unity-gain bandwidth are noticeably enhanced with introducing an under-weak-inversion gain-stage in the Miller capacitor feedback path [14].

This paper is organized as follows. Section II mentions the conventional right half-plan (RHP) zero controlling techniques. In section III, the proposed architecture is presented while compared with normal Miller compensation. Section IV presents the simulation results and makes a comparison between this work and other ultra-low-power low-frequency OTAs, followed by section V concluding the paper.

II. Conventional RHP Zero Controlling Techniques

Clearly, a disadvantage of the Miller frequency compensation technique is the inconvenience of the right half-plane (RHP) zero. This RHP zero degrades the phase margin and leads to instability of operational amplifiers. Two different approaches of controlling the RHP zero are shown in Fig. 1 [15]. As observed in Fig. 1 (a), the nulling resistor controls the RHP zero by the basis of displacement. On the other hand, as shown in Fig. 1 (b), the employed gain-stage M2 prevent the input current from going directly through the Miller capacitor, thus, the RHP zero will eliminate [16].

In a way, a tradeoff exists in implementing the nulling resistor $R$, shown in Fig. 1 (a) in ultra-low-voltage conditions. In case of implementing $R$, in form of an active resistor, it may be difficult to provide the required bias voltage. On the other hand, if $R$ implements as a passive resistor, it degrades the total area.

As can be observed in Fig. 1 (a), at frequencies near unity-gain frequency, the reactance of the compensation
capacitor $C_c$ can be ignored. Therefore, the output resistance seen by $C_{out}$ can be derived as given by

$$R_{out} \approx \frac{1}{g_{m1}}$$  \hspace{1cm} (1)$$

while from Fig. 1 (b), the output resistance seen by $C_{out}$ can be expressed as [15]

$$R_{out} \approx \frac{1}{g_{m1}(g_{m2}^2r_{ds2})}$$  \hspace{1cm} (2)$$

And also,

$$p_o = \frac{1}{R_{out}C_{out}}.$$  \hspace{1cm} (3)$$

Obviously, it can be deduced from (2) and (3) that noticeable reduction of $R_{out}$ by a factor of $g_{m2}^2 r_{ds2}$ is the basis of improvement in “pole-splitting” effect which is valid only for Fig. 1 (b) and not for Fig. 1 (a). Therefore, increasing the magnitude of the non-dominant output pole $p_o$, mainly due to the employed gain-stage $M_2$, leads to a proportional enhancement in unity-gain bandwidth.

### III. Proposed Architecture

According to the expressions that are derived from the model BSIM3v3 in weak inversion [17], the drain current of a MOS transistor can be presented by

$$I_{DS} = I_s \left\{ \frac{W}{L} \right\} \exp \left( q \frac{V_{GS} - V_{TH}}{nKT} \right) \left[ 1 - \exp \left( -q \frac{V_{DS}}{KT} \right) \right]$$  \hspace{1cm} (4)$$

Where $I_s$ is the characteristic current, $q$ is the charge of the electron or hole, $n$ is the inclination of the curve in weak inversion, $k$ is the Boltzman constant and $T$ is the absolute temperature. The transconductance $g_{m}$ and $g_{mb}$ can be found as presented in (5) and (6) respectively, where $\gamma$ is the body effect coefficient and $\phi_F$ is the Fermi potential [15].

$$g_m = \frac{I_{DS}}{nKT}$$  \hspace{1cm} (5)$$

$$g_{mb} = \frac{\gamma}{2\sqrt{2\phi_F-V_{SB}}} g_m$$  \hspace{1cm} (6)$$

The presented architecture based on a bulk-driven input differential pair is illustrated in Fig. 2 [14], which allows a large input signal swing. Due to the extremely low currents in ultra-low-power condition, it can be deduced from (5) and (6) that the DC gain as a function of $g_m$ and $g_{mb}$ can be limited. However, in this work, the employed under-weak-inversion gain-stage $M_6$ that has been added to the Miller capacitor feedback path to increase the UGBW, enhances the DC gain as well because of the “cascode” technique effect.
Consequently, the gain-bandwidth product (GBW) was remarkably enhanced.

As observed in Fig. 2, the compensation result is to keep the dominant pole roughly the same as normal Miller compensation and to increase the output pole by approximately the gain of a single stage $M_6$. As mentioned in section II, under weak inversion, the magnitude of the output pole can be given by

$$\frac{g_{m6}}{C_{out}}\approx \frac{g_{m12}(g_{m6}+g_{mb6})r_{ds6}}{C_{out}}$$

(7)

Where $g_{m6}$ and $g_{mb6}$ are the transconductances of $M_6$ and presented in (5) and (6) respectively. Consequently, the output pole has split from the dominant pole by a factor of $(g_{m6}+g_{mb6})r_{ds6}$ which leads to an enhancement in unity-gain bandwidth, when compared to the nulling resistor approach.

As discussed in [13], slew rate can be achieved with a complex approach because input transistors $M_1$ and $M_2$ will never become cut off and the current of $M_{13}$ never flows in just one of them. In this work, from the expressions in relation with the compensation capacitor $C_c$, the slew rate is given by

$$SR = \frac{I_{DS2}-I_{DS1}}{C_c}.$$  

(8)

Therefore, slew rate can be obtained from the operating point analysis given by the simulations.

Considering Fig. 2, transistor pairs $M_7-M_9$ and $M_8-M_{10}$ form “composite transistors”. In terms of dc analysis, the drain-source voltage of transistor $M_9$ is given by (9). An analogous expression is achieved for $V_{DS10}$.

$$V_{DS9} = \frac{KTL}{q} \left[ \ln \left( 1 + \frac{W}{L} \right) \right]$$

(9)

Consider that $V_{DS9}$ does not depend on the gate-source voltage, which is valid only for weak inversion and not for strong inversion [13]. In order that $V_{DS9}$ and $V_{DS10}$ are equal, $V_{DS1}$ and $V_{DS2}$ should be equal and constant. Therefore, the differential offset voltage of input transistors will reduce [13].

In order to avoid any systematic offset it is possible to derive an equation as follows.

$$V_{GS12} = V_{DS10} + V_{DS8} \quad V_{GS9} = V_{DS9} + V_{DS7}$$

(10)

So,

$$V_{GS12} = V_{GS9}$$

(11)

With respect to (11) we can write

$$I_{DS9} = \frac{(W/L)_{10}}{(W/L)_{12}} I_{DS12} = I_{DS3} + \frac{I_{DS13}}{2}$$

(12)

Therefore, slew rate can be obtained from the operating point analysis given by the simulations.
Therefore,

\[
\left(\frac{W}{L}\right)_{12} = \frac{2\left(L/W\right)_9 \left(L/W\right)_{11}}{2\left(L/W\right)_3 + \left(L/W\right)_{13}}.
\]

(13)

There will be no systematic offset voltage as long as (13) is satisfied.

Although, the weak inversion operation implies large transistors dimensions, it minimizes the noise effect, especially flicker noise which is important in a MOS transistor in low-frequency applications [15].

IV. Simulation Results

The circuit was simulated in HSPICE with BSIM3v3.1 model based on a standard 0.18 μm CMOS process \((V_{DD} = 0.45 \text{ V}, V_{PP} = -0.5 \text{ V})\). Simulations resulted on considerable increase of unity-gain bandwidth to the value of 83.88 KHz, the improved DC gain of 88.5 dB, and a phase margin of 66.3° (see Fig. 3). The presented topology employed weak inversion transistors is capable of working at 500 mV of power supply with full rail-to-rail input and output swings and consuming only 1.02 μW. The reference current of the improved OTA, \(I_{ref}\), was set equal to 130 nA. Additionally, with the large load capacitor \(C_L\) of 15 pF and with a compensation capacitor \(C_C\) of 5 pF, the slew rate of 52 V/μs is resulted (see Fig. 4).

Table 1 shows a comparison with other low-voltage and low-frequency operational amplifiers to evaluate this work using a figure of merit (FoM) defined as

\[
\text{FoM} = \frac{(\text{Gain})(\text{Unity gain freq.})}{(\text{Power supply})(\text{Power consumption})},
\]

(14)

The proposed architecture shows a noticeable FoM even under the condition of ultra low supply voltage of 500 mV.

V. Conclusion

This work proposed an improved 0.5-V ultra-low-power OTA based on a bulk-driven input differential pair and employed an under-weak-inversion gain-stage in the Miller capacitor feedback path. This paper successfully demonstrated an alternative low-area approach without the use of additional circuit or extra power consumption. Simulation results have been presented to confirm the considerable improvement in the unity-gain bandwidth and also the DC gain, when compared to other ultra-low-power low-frequency OTAs with conventional RHP zero controlling techniques. The presented topology allows rail-to-rail input and output swings at 500-mV of power supply, therefore, it works beyond the limit given by the threshold voltages.

References

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Authors’ information

1-IC Design Lab., Department of Electronics, Sadjad Higher Education Institution.

Milad Razzaghpour was born in Mashhad, Iran, on August 22, 1986. He received the B.Sc. degree in electrical engineering from Sadjad Higher Education Institution, Mashhad, Iran, in 2008. From 2006 to 2009, he was a Research Assistant at Sadjad Research Center, Mashhad, Iran. His research interests include CMOS analog integrated circuit design, computer-aided design of VLSI systems and neural networks. He is a student member of IEEE.

Abbas Golmakani was born in Mashhad, Iran, on December 3, 1974. He received the B.Sc. and M.Sc. degree in electrical engineering from Sharif University of Technology, Tehran, Iran, in 1996 and 1998, respectively. Since 1999, he has been with Department of Electronics, Sadjad Higher Education Institution, Mashhad, Iran. Since 2005, he has been working toward the Ph.D. degree in the Department of Electronics, Ferdowsi University of Mashhad, Mashhad, Iran. His research interests include CMOS analog and RF circuit design.